REMARKS

Prior to entry of this paper, Claims 1-20 were pending. Claim 5 was objected to, but identified as being allowable if re-written in independent form. Claims 1-4 and 6-20 were rejected. In this paper, Claims 1, 4, 5, 7, 9, 12, 13, 14, 16, and 20 are amended. Claims 5, 9, and 12 are amended to be re-written in independent form. Claim 7 was amended for consistency with the amendment to Claim 1. Claim 14 was amended for consistency with the amendment to Claim 13. Claims 4 and 16 are amended based on intervening change in case law presented by SuperGuide Corporation v. DirecTV Enterprises, Inc., et al., 358 F.3d 870 (Fed. Cir. 2004), and the amendments to Claims 4 and 16 do not narrow the scope of Claims 4 and 16. Claims 1-20 are currently pending. In this paper, whenever language is quoted from a claim that has been amended with regard to portion of the claim quoted, the quoted claim language is that of the claim as amended. No new matter is added by way of this amendment. For at least the following reasons, Applicants respectfully submit that each of the presently pending claims is in condition for allowance.

Allowable Subject Matter (Claim 5)

Claim 5 was identified as being allowable if re-written in independent form. In this paper, Claim 5 is re-written in independent form. For at least this reason, it is respectfully submitted that Claim 5 is in condition for allowance.

Claims 1-4, 6-8, 11, and 13-20

Claims 1, 13 and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by Jackson et al (U.S. Publication No. 2002/0067773), hereinafter "Jackson et al."

Claim 1 is respectfully submitted to be allowable at least because Jackson fails to disclose, "the synthesized signal is a clock signal", as recited in Applicants' Claim 1. The signal output by VCO 64 of FIG. 3 of Jackson is a sinusoidal signal, not a clock signal.

Claims 2-4, 6-8, and 11 are respectfully submitted to be allowable at least because they depend from Claim 1. Claim 13 and 20 are respectfully submitted to be allowable at least for reasons similar to those stated above with regard to Claim 1. Claims 14-19 are respectfully submitted to be allowable at least because they depend from Claim 13.

Claims 9-10

Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson. This rejection is respectfully traversed. Claim 9 is respectfully submitted to be allowable at least because Jackson fails to disclose, teach, or suggest, "a clock divider circuit that is configured to provide an output clock signal from the synthesized signal", as recited in Applicants' Claim 9.

The Office Action states, "As to claims 9 and 18, Jackson et al teaches a clock divider that is configures to provide an output clock signal from the synthesized signal in (Figure 1)." However, in the circuit of Figure 1 of Jackson, the synthesized signal (the output of VCO 18) is a provided directly as the output signal; there is no clock divider or other circuit modifying the synthesized signal prior to providing it as the output signal. Additionally, in the circuit of Figure 1 of Jackson, the output signal is a sinusoidal signal, not a clock signal. There is a frequency divider 12 in the circuit of Figure 1 of Jackson, but the frequency signal is not a clock divider because neither its input nor its output is a clock signal; rather, its input is a sinusoidal signal and its output is a sinusoidal signal.

For at least this reason, it is respectfully submitted that Claim 9 is in condition for allowance.

Claim 10 is respectfully submitted to be allowable at least because it depends from Claim 9.

Claim 12

Claim 12 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Jackson et al in view of Leung et al (U.S. Patent No. 6,580,432), hereinafter "Leung."

The rejection is respectfully traversed, at least because the proposed modification would render the circuit of Jackson unsuitable for its intended purpose.

The Office Action states, "Jackson et al fails to teach the modulating waveform is suitable for spreading a frequency spectrum that is associated with the synthesized signal relative to a frequency spectrum that is associated with the reference signal according to a downspread modulation. However, Leung does teach this feature". However, it is the modulating waveform of Leung that accomplishes downspread modulation, not the modulating waveform of Jackson. In Jackson, QPSK modulation is performed. QPSK modulation modulates the frequency of a carrier signal. In QPSK modulation, the frequency modulation is performed to encode digital data. Accordingly, in QPSK modulation, data is encoded in the frequency of the output signal.

However, in Leung, frequency modulation is performed for reducing EMI. In Leung, the frequency modulation is done in a specific way to reduce EMI. In QPSK modulation, frequency modulation is performed to encode data. If Jackson were modified so that the frequency modulation was done in the manner taught in Leung, then the frequency modulation would no longer encode digital data. This is contrary to the purpose of the circuit of Jackson, which is to encode digital data by modulating the frequency.

Accordingly, the proposed modification would render the circuit of Jackson unsuitable for its intended purpose.

For at least this reason, it is respectfully submitted that Claim 12 is in condition for allowance.

Further, the section of Leung quoted by the Office refers to downspread modulation accomplished by shifting the carrier frequency down by half of the modulation amount, and also notes that "One advantage of downspreading is that is [sic] can insure that a system does not exceed

the maximum processor's clock speed." The Office Action states, "Therefore, taking Jackson et al and Leung et at as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teaching to include downspread modulation at taught by Leung so that the entire system does not exceed the maximum processor's clock speed."

Applicant respectfully disagrees with this as a reason to modify the frequency of Jackson. The circuit of Leung provides a clock signal that is used to clock a processor. Obviously, reducing the frequency of this clock signal in Leung would help ensure that the entire system does not exceed the maximum processor's clock speed. However, the circuit of Jackson provides a sinusoidal signal, an analog signal that is encoded with digital data in its frequency. The frequency of the signal output by the circuit of Jackson would have no effect on processor clock speed and reducing the frequency of the signal output by Jackson would not ensure that that a maximum processor clock speed is not exceeded.

CONCLUSION

It is respectfully submitted that each of the presently pending claims (Claims 1-20) is in condition for allowance and notification to that effect is requested. Examiner is invited to contact the Applicants' representative at the below-listed telephone number if it is believed that the prosecution of this application may be assisted thereby. Although only certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentable. Applicant reserves the right to raise these arguments in the future.

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Respectfully submitted,

By _____

Matthew M. Gaffney
Registration No.: 46,717
DARBY & DARBY P.C.
P.O. Box 770
Church Street Station
New York, New York 10008-0770
(206) 262-8910
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant